Cycle To Cycle Jitter Of CPU Clocks

Evaluating Multi-Frequency Clock Distribution Circuits

Current microprocessor based systems employ clock distribution systems that incorporate multiple, Phase Locked Loop (PLL) based frequency multipliers. Figure 1 shows a block diagram of a typical clock distribution system. The master clock is a 16 MHz crystal oscillator. A PLL based frequency multiplier/buffer doubles the clock frequency and provides multiple buffered outputs. The resulting 32 MHz clock is then distributed throughout the system. The central processor (CPU) uses this clock and internally multiplies the frequency by 3 for internal operations.

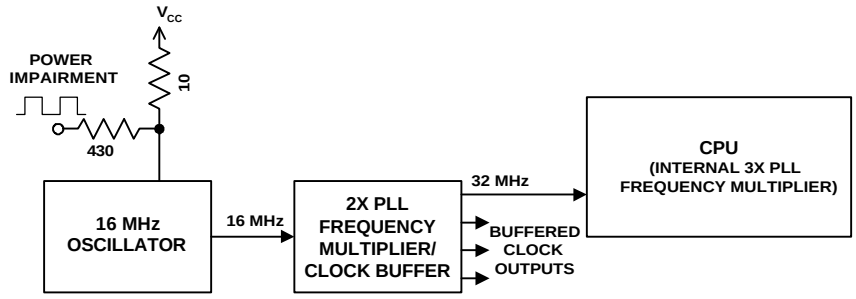

Figure 1 – Block diagram of a phase locked loop based multi-frequency clock distribution circuit

Timing problems can develop if the jitter of any of the clock stages exceeds the maximum slew rate limit for the following PLL multiplier. Such a fault could lead to loss of lock and a disruption of the clock signal. Jitter is the deviation of the clock timing from its ideal value. Cycle to cycle jitter is the instantaneous difference of period between adjacent clock cycles and measures the slew rate of the clock. Cycle to cycle jitter is diagramed in figure 2.

LeCroy oscilloscopes offer an optional Jitter and Timing Analysis (JTA) package that includes 7 parameters and 6 functions for measuring jitter. These include cycle to cycle, period, width, duty cycle, frequency, and interval error jitter. The parameters can be histogrammed for detailed statistical analysis. These tools are extremely useful in verifying critical circuit timing in multi-frequency clock systems.

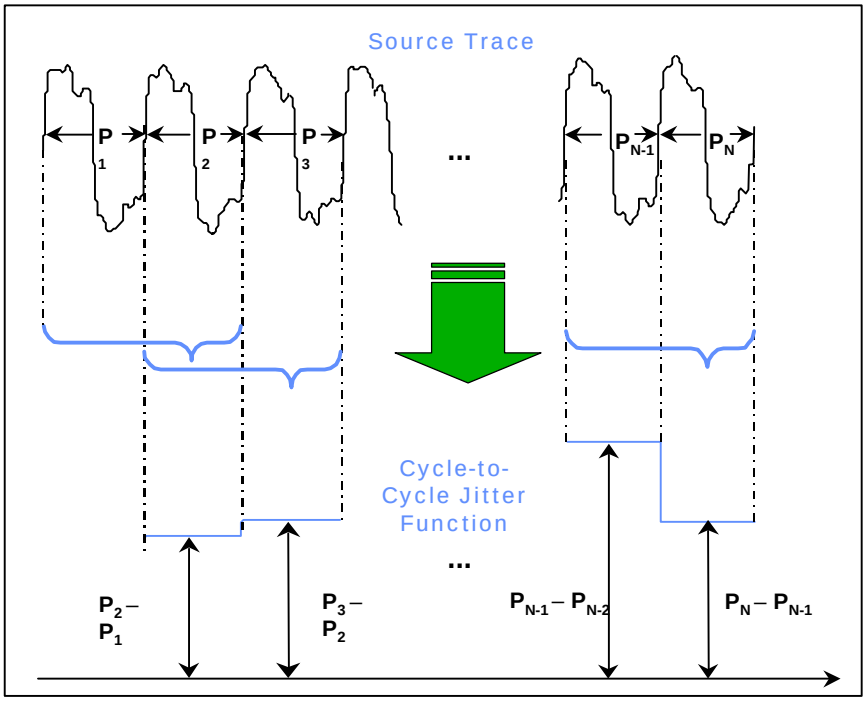

Figure 2 Details of the cycle to cycle JitterTrack measurement

Figure 3 shows the result of a study of the effects of power supply ripple on the clock system. A square wave, shown in the lower trace (CH3) in the figure, is applied via a voltage divider, shown in figure 1, to the power input of the master oscillator. This results in 120 mV of peak to peak ripple at the supply terminal of the oscillator. The output of the oscillator is acquired in trace 2 at the top of the figure. The cycle to cycle jitter function (Jcy-cy) is shown in trace A. This signal is averaged synchronously (trace B) with the injected ripple waveform to enhance the jitter components due to the ripple. Note that cycle to cycle jitter increases at the same time the square wave transitions. These are the most significant cycle to cycle jitter events.

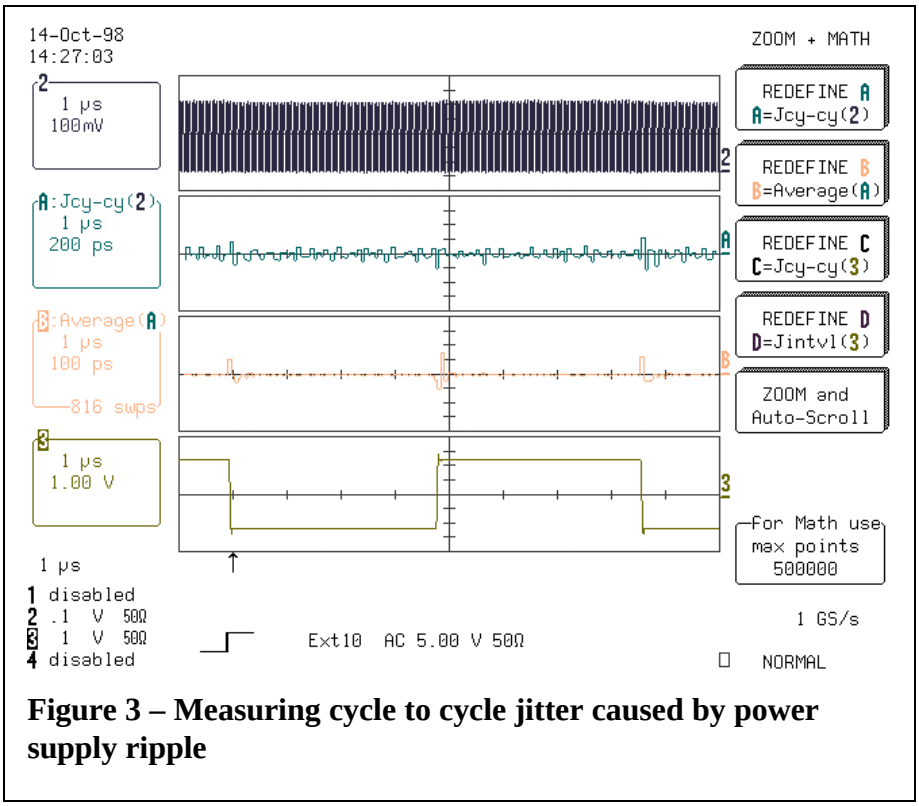

Figure 3 – Measuring cycle to cycle jitter caused by power supply ripple

Trace C in figure 4 shows the cycle to cycle jitter measured at an output of the X2 frequency multiplier. This PLL based device shows a higher level of cycle to cycle jitter. Trace D displays the time interval error of the frequency multiplier. This function plots the time difference between each edge and an ideal clock period specified by the user as shown in the setup menu. For a fixed frequency clock this corresponds to instantaneous phase error. Note that the frequency multiplier phase error tracks the ripple waveform. As can be seen it is possible to track timing effects through the entire clock system using tools found in the jitter and timing analysis option.

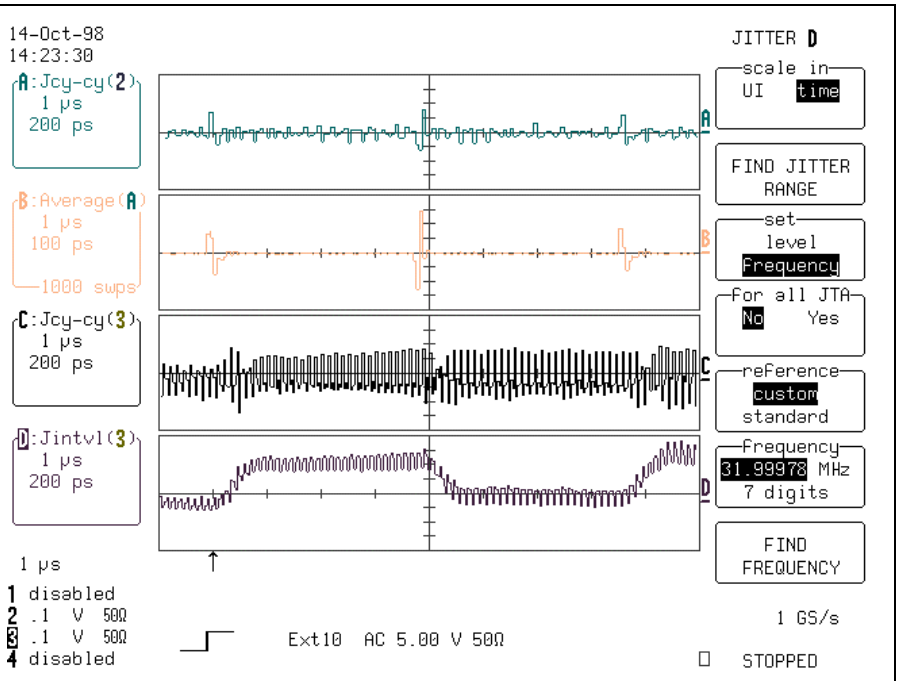

Figure 4 – Comparing oscillator and multiplier jitter